

ABSTRACT OF THE DISCLOSURE

The present invention relates generally to data processing systems, in particular, to high speed data communication and chip-to-chip data transfer.

5 The data transferring apparatus comprises:

a data input and data output;

a plurality of data transferring sections operable in parallel for transferring data as data words having bit width which is a multiple M of the bit width of the input data and a circuit for synchronising said parallel data transferring sections;

10 a programmable frequency clock generator for generating a clock signal, said programmed frequency including a full-frequency and low-frequency, the low frequency being equal to quotient of the full frequency divided by and the number of said data transferring sections;

15 wherein said data transferring sections operate at said low frequency; while said input and output data are provided at said full frequency.

Preferably, the data transferring apparatus further comprises a multiplexer that receives wide data words from said data transferring sections at said low frequency and provides multiplexed output data at said full frequency.

20 The invention is particularly applicable to computer-controlled automatic test systems for testing integrated circuits, more particularly, to memory test systems which interface with high speed protocol memories such as synchronous DRAM, in particular DDR.